IN THE CLAIMS

Claim 1 (Currently Amended): An apparatus comprising:

a host controller; and

a host controller driver,

wherein a plurality of banks containing a plurality of queue element transfer descriptors (qTDs) are created for a plurality of buffers posted to the host controller driver, ~~and~~ the qTDs are circularly linked, and at least one qTD of the plurality of qTDs operates to store overflow content ~~of at least one~~in a first buffer of the plurality of buffers when execution of the contents of the first buffer is completed without a short packet condition when a size of the contents in the first buffer is greater than a storage capacity in a first bank of the plurality of banks.

Claim 2 (Original): The apparatus of claim 1, wherein the host controller is an enhanced host controller interface (EHCI) host controller.

Claim 3 (Original): The apparatus of claim 1, wherein the banks are associated with a particular buffer in the plurality of buffers.

Claim 4 (Original): The apparatus of claim 3, wherein the plurality of buffers are ordered in an incremented order.

Claim 5 (Original): The apparatus of claim 4, wherein a second buffer is executed upon an occurrence of a short packet in a first qTD associated with a first buffer, the first qTD having an alternate next pointer pointing to a first qTD of the second buffer.

Claim 6 (Original): The apparatus of claim 1, wherein a next pointer in each of the plurality of qTDs in a first bank point to a next qTD in the first bank, a last qTD in the first bank points to a first qTD in the first bank.

Claim 7 (Currently Amended): An apparatus comprising:

a host controller; and

a host controller driver coupled to the host controller,

wherein the host controller arranges queue element transfer descriptors (qTDs) in a circularly linked order, ~~and~~ at least one qTD operates to store overflow content ~~of at least one~~in a first buffer of a plurality of buffers when execution of the contents of the first buffer is completed without a short packet condition when a size of the contents in the first buffer is greater than a storage capacity in a first bank of the plurality of banks.

Claim 8 (Original): The apparatus of claim 7, wherein a plurality of banks containing a plurality of qTDs are created for the plurality of buffers posted to the host controller driver.

Claim 9 (Original): The apparatus of claim 7, wherein the host controller is an enhanced host controller interface (EHCI) host controller.

Claim 10 (Original): The apparatus of claim 8, wherein the banks are associated with a particular buffer in the plurality of buffers.

Claim 11 (Original): The apparatus of claim 10, wherein a second buffer is executed upon an occurrence of a short packet in a first qTD associated with a first buffer, the first qTD having an alternate next pointer pointing to a first qTD of the second buffer.

Claim 12 (Original): The apparatus of claim 8, wherein a next pointer in each of the plurality of qTDs in a first bank point to a next qTD in the first bank, a last qTD in the first bank points to a first qTD in the first bank.

Claim 13 (Currently Amended): A system comprising:

a bus;

a first host controller coupled to the bus; and

a second host controller coupled to the first host controller;

wherein the first host controller arranges queue element transfer descriptors (qTDs) in a circularly linked order and at least one qTD operates to store overflow content ~~of at least one~~in a first buffer a plurality of buffers when execution of the contents of the first buffer is completed without a short packet condition when a size of the contents in the first buffer is greater than a storage capacity in a first bank of the plurality of banks.

Claim 14 (Original): The system of claim 13, wherein a plurality of banks containing a plurality of qTDs are created for the plurality of buffers posted to a host controller driver.

Claim 15 (Original): The system of claim 13, wherein the first host controller is an enhanced host controller interface (EHCI) host controller.

Claim 16 (Original): The system of claim 14, wherein the banks are associated with a particular buffer in the plurality of buffers.

Claim 17 (Original): The system of claim 16, wherein a second buffer is executed upon an occurrence of a short packet in a first qTD associated with a first buffer, the first qTD having an alternate next pointer pointing to a first qTD of the second buffer.

Claim 18 (Original): The system of claim 13, wherein a next pointer in each of the plurality of qTDs in a first bank point to a next qTD in the first bank, a last qTD in the first bank points to a first qTD in the first bank.